REMARKS

Applicants have studied the Office Action dated March 15, 2006 and have made amendments to claims 1-2, 7-9, 14-15, and 21-22. No new matter was added. Reconsideration and allowance of the pending claims in view the following remarks are respectfully requested. Applicant submits that the application, as amended, is in condition for allowance. In the Office Action, the Examiner:

- Rejected claims 1-22 under 35 U.S.C § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention;
- Rejected claims 1, 3, 7-10, 14-17, and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Applicant admitted prior art ("AAPA"); and
- Rejected claims 2, 4-6, 11-13, and 18-20 under 35 U.S.C. § 103(a) as being unpatentable over Applicant admitted prior art ("AAPA") as applied to claim 1, and further in view of Guo et al. ("A Technique for Fault Diagnosis of Defects in Scan Chains", IEEE, 2001, ITC international test conference, pager 10.2, pgs. 268-277).

Rejection Under 35 U.S.C. § 112

As noted above, the Examiner rejected claims 1-22 under 35 U.S.C § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the Examiner states that the preamble of claims 1, 8, 15, and 21-22 recites "method of identifying one or more defective shift register latches in a scan chain", but the body of the claims do not include a corresponding step.

Although the Applicant respectfully disagrees with the Examiner that a claim is required to have a step corresponding with the preamble especially since the body of claims 1, 8, 15, and 21-22 recite how to identify a defective latch, the Applicant has amended

claims 1, 8, 15, and 21-22 to further prosecution. Claims 1, 8, 15, and 21-22 now recite" identifying at least one defective shift register latch in the scan chain circuit. Therefore, the Applicant believes that the Examiner's rejection has been overcome and should be withdrawn.

Rejection under 35 U.S.C. §103(a) as being unpatentable over Applicant Admitted Art

As noted above, the Examiner rejected claims 1, 3, 7-10, 14-17, and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Applicant admitted prior art ("AAPA"). The Examiner recites 35 U.S.C. §103. The Statute expressly requires that obviousness or non-obviousness be determined for the claimed subject matter "as a whole," and the key to proper determination of the differences between the prior art and the present invention is giving full recognition to the invention "as a whole." The Applicant Admitted Prior Art take simply does not suggest, teach, or disclose the patentably distinct limitations of:

> placing the scan chain circuit into an operating region;
>
> loading a scan test pattern into the scan chain circuit;
>
> placing the scan chain circuit into a failing region;
>
> applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the falling region;
>
> placing the scan chain circuit into an operating region;
>
> unloading the scan chain circuit; and
>
> identifying at least one defective shift register latch in the scan chain circuit.

With respect to claims 1 and 22, the Examiner states that the AAPA teaches "applying a shift clock pulse to the clock input of the second latch" and directs the Applicant to lines 9-10 of paragraph [0007] of the Specification as originally

filed. The Applicant has amended claims 1, 8, 15, and 21-22 to more clearly recite:

> applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the failing region

Support for this amendment is found at FIG. 8 and in paragraph [0040] of the Specification as originally filed.

Paragraph [007], where the Examiner directs the Applicant, merely states "the logical value that is present on the L1 Output 312 is stored into latch L2 318 upon a transition of shift clock "b" 314 (or shift clock c2) from a logical low level to a logical high level". Nowhere does the AAPA state that the scan chain is placed into a failing region and then a shift clock pulse is applied to the clock input of the second latch while the scan chain circuit is in the falling region. Furthermore, nowhere does the AAPA state that the scan chain is placed in a failing region where a shift clock pulse is applied and placing the scan chain into an operating region. Accordingly, the presently claimed invention distinguishes over the APPA for at least these reasons.

The Examiner goes on to separate claim 1 into two separate methods, the first method being "placing the scan chain circuit into an operating region; loading a scan test pattern into the scan chain circuit; placing the scan chain circuit into a failing region; applying a shift clock pulse to the clock input of the second latch", and the second method being "placing the scan chain circuit into an operating region; unloading the scan chain". The Applicant respectfully reminds the Examiner that a claim is to be considered as a whole, with each claim element being considered in light of every other claim element.

The Examiner correctly states that the AAPA "does not disclose the combination of these two methods. However, the AAPA, lines 4-6 of paragraph (0016) discloses that a third defect or inner defect can be detected by either separately or combined of these

methods. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to combine the first and second methods into one method steps so that multiple defects can be detected".

However, the Applicant respectfully disagrees. Paragraph [0016] where the Examiner directs the Applicant was inadvertently mistyped. The Applicant has amended claim [0016] to now more clearly recite:

> When there are multiple DC defects in a scan chain, only the first and last defect in the scan chain can be diagnosed and identified using the two mentioned methods. Although this is useful, if there are multiple defects, for example a third defect at RML 3 which is between defect 652 of RML4 and defect 654, ~~This~~ this third defect or inner defect (inner meaning after the first and last defect of a chain) ~~is to~~ cannot be detected by these prior art methods, either separately or combined. Further any multiple defects that occur between a first defect and a last defect are not detected by these prior art method either, again either separately or combined

Paragraph [0016] originally recited "which is between defect 652 of RML4 and defect 654 This third defect or inner defect (inner meaning after the first and last defect of a chain) is to be detected by these prior art methods, either separately or combined". As can be seen, a portion of paragraph [0016] originally comprised typographical and grammatical errors. Furthermore, the preceding section of paragraph [0016] recites "When there are multiple DC defects in a scan chain, only the first and last defect in the scan chain can be diagnosed and identified using the two mentioned methods", which clearly shows the intention of the Applicant to state that the two methods cannot detect inner defects. The next sentence further states, "Although this is useful', meaning that although the two methods are useful for identifying the first and last defect, the two methods cannot detect inner defects either alone or in combination. The following sentence further shows the Applicant's intention by reciting "Further any multiple defects that occur between a first defect and a last defect are not detected by these prior art method either, again either separately or combined".

Therefore, the revised section or paragraph [0016], which recites "Although this is useful, if there are multiple defects, for example a third defect at RML 3 which is between defect 652 of RML4 and defect 654, this third defect or inner defect (inner meaning after the first and last defect of a chain) cannot be detected by these prior art methods, either separately or combined" does not constitute new matter and clearly shows that the two methods cannot determine inner defects alone or in combination. Accordingly, the combination of "placing the scan circuit into an operating region...placing the scan chain circuit into a failing region...." is not rendered obvious by the AAPA. Therefore, the presently claimed invention distinguishes over the AAPA for at least these reasons as well.

The Examiner rejects claims 8, 15, and 21-22 under the same rational as set forth for claim 1. However, the Applicants respectfully bring to the Examiner's attention that claims 8, 15, and 22 include different claim elements than claim 1. For example, claim 8 recites "...applying a scan clock pulse to the clock input of the first latch...placing the scan chain circuit into an operating region; applying a shift clock pulse to the clock input of the second latch...". This combination of claim elements is not included in claim 1.

The arguments and remarks made above with respect to claim 1 are also applicable to claim 8 as well. However, the Applicant has amended claim 8 to more clearly recite "applying a scan clock pulse to the clock input of the first latch, wherein the scan clock pulse is applied while the scan chain circuit is in the failing region; placing the scan chain circuit into an operating region; applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the operating region". The application of a shift clock pulse allows for a "skewed" unload to be performed. See paragraph [0041] of the Specification as originally filed. Nowhere does the AAPA state that a scan clock pulse "is applied while the scan chain circuit is in the failing region" and that a shift clock pulse "is applied while the scan chain circuit is in the operating region". Accordingly the presently claimed invention distinguishes over the AAPA for at least these reasons as well.

With respect to claims 15 and 22, the arguments and remarks made above with respect to claim 1 are likewise applicable. However, claims 15 and 22 further recite "...placing the scan chain circuit into a failing region; applying a scan clock pulse to the clock input of the first latch; applying a shift clock pulse to the clock input of the second latch" The Applicant has amended claims 15 and 22 to more clearly recite "applying a scan clock pulse to the clock input of the first latch, wherein the scan clock pulse is applied while the scan chain circuit is in the failing region; applying a shift clock pulse to the clock input of the second latch, wherein the shift clock pulse is applied while the scan chain circuit is in the failing region". Nowhere does the AAPA state that a scan clock pulse is applied to the first latch while the scan chain is in the operating mode and that a shift clock pulse is applied to the second latch while scan chain is in the operating mode. Accordingly, the presently claimed invention distinguishes over the AAPA for at least these reasons.

Support for the amendments made to claims 15 and 22 can be found in the Specification as originally filed at paragraphs [0040] and [0041]. No new matter has been added.

For the foregoing reasons, independent claims 1, 8, 15, and 21-22 distinguish over the AAPA. Claims 3, 7, 9-10, 14, 16-17, depend from independent claims 1, 8, and 15 respectively. Since dependent claims contain all the limitations of the independent claims, claims 3, 7, 9-10, 14, 16-17 distinguish over the AAPA, as well, and the Examiner's rejection should be withdrawn. However, additional arguments are given below with respect to claims 7 and 14.

The Examiner states that the AAPA teaches at paragraph [0007] the following element of claims 7 and 14: "applying a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch". However, the Applicant respectfully disagrees. The Applicant has amended claims 7 and 14 to more clearly recite "applying

a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch, wherein the scan pulse and the shift clock pulse are applied while the scan chain is in the operating region". By applying the scan pulse and the shift clock pulse in pairs, the presently claimed invention identifies defects and/or errors in both the L1 and L2 latches simultaneously. See the Specification as originally filed at paragraph [0047]. Nowhere does the AAPA state that the "the scan pulse and the shift clock pulse are applied while the scan chain is in the operating region". The AAPA merely states that "the logical value that is present on the L1 Output 312 is stored into latch L2 318 upon a transition of shift clock "b" 314 (or shift clock c2) from a logical low level to a logical high level. After the L1 Output 312 is stored into the L2 latch or slave latch 318 that logic value is available, after a propagation delay, on the L2 output 320". Accordingly, the presently claimed invention distinguishes over the AAPA for at least these reasons as well.

Rejection under 35 U.S.C. §103(a) as being unpatentable over AAPA and Guo et al.

As noted above, the Examiner rejected claims 2, 4-6, 11-13, and 18-20 under 35 U.S.C. §103(a) as being unpatentable over the AAPA as applied to claim 1, and further in view of Guo et al. ("A Technique for Fault Diagnosis of Defects in Scan Chains", IEEE, 2001, ITC International test conference, pager 10.2, pgs. 268-277).

The arguments and remarks made above with respect to claims 1, 8, and 15 are likewise applicable here and will not be repeated. Furthermore nowhere does Guo teach the claim elements of claims 1, 8, and 15 discussed above. For the foregoing reasons, independent claims 1, 8, and 15 distinguish over the AAPA taken alone and/or in combination with Guo. Claims 2, 4-6, 11-13, and 18-20 claims depend from claims 1, 8, and 15 respectively. Since dependent claims contain all the limitations of the independent claims, claims 3, 7, 9-10, 14, 16-17 distinguish over the AAPA taken alone and/or in combination with Guo, as well, and the Examiner's rejection should be withdrawn.

CONCLUSION

Applicants acknowledge the continuing duty of candor and good faith to disclosure of information known to be material to the examination of this application. In accordance with 37 CFR § 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment is limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

Applicants respectfully submit that all of the grounds for rejection stated in the Examiner's Office Action have been overcome and that all claims in the application are allowable. No Previously Presented matter has been added. It is believed that the application is now in condition for allowance or alternatively is in better form for consideration on appeal, which allowance is respectfully requested.

PLEASE CALL the undersigned if that would expedite the prosecution of this application.

Respectfully Submitted,

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